UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/519,187	12/22/2004	Satoshi Funada	0670-7051	6815

31780 7590 09/17/2008

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
NOONAN, WILLOW W	

ART UNIT	PAPER NUMBER
2146	

MAIL DATE	DELIVERY MODE
09/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,187	FUNADA, SATOSHI	
	Examiner	Art Unit	
	WILLOW NOONAN	2146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/814,821 has a total of 9 claims pending in the application; there are 5 independent claims and 4 dependent claims, all of which are ready for examination by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 15-23 are rejected under 35 U.S.C. 102 as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over **Rompaey** (U.S. Patent No. 5,870,588)

Regarding claim 15, Rompaey teaches an information processing apparatus comprising a plurality of hardware circuit blocks, each configured so as to implement one of functional units of certain information processing software as hardware, the plurality of hardware circuit blocks mutually operating in pipeline. *See* Rompaey at col. 6, lines 57-70 (“In another aspect of the present invention, the aspects comprise any one or more of functional, communication, concurrency and structural aspects of the digital system. The objects representing the functional aspects comprise any one or

more of host language encapsulations, threads, and context"). Rompaey teaches that each of the plurality of hardware circuit blocks comprises:

a first processing circuit module connected to a memory for operating to selectively make read access or write access to the memory in response to the input of packet data and on the basis of the content of the packet, *see* Rompaey at fig. 10;

a second processing circuit module for operating to receive packet data outputted from the first processing module to create packet data obtained by subjecting a predetermined information process to the received packet, *see* Rompaey at fig. 10; and

an interface module for operating to receive input packet data to each hardware circuit block and the packet data created by the second processing circuit module to provide these received packet data to the first processing circuit module at separate timing, *see* Rompaey at col. 6, lines 18-34 (describing how hierarchal objects combine primitive components),

wherein the first processing circuit module responds to either one of the input packet data provided via the interface circuit module and the packet data subjected to the predetermined information process so that when responding to the input packet data the first processing circuit module reads out of the memory information data needed to process the input packet data and when responding to the packet data subjected to the predetermined information process the first processing circuit module writes new information data associated with that packet data into the memory while causing each hardware circuit block to output the packet data subjected to the predetermined

information process, *see* Rompaey at p. 13, paragraph 3 ("A protocol may further have an index set. The indices in the index set are used to convey extra information about the data that is transported. For example the primitive protocol used to model the memory port of a processor will have an index to model the address of the data that is put on the memory port").

Regarding claim 16, Rompaey teaches an information processing apparatus comprising a plurality of hardware circuit blocks each of which functions to output packet data by subjecting a specific information process to given input packet data, the plurality of hardware circuit blocks mutually operating in pipeline. *See* Rompaey at col. 6, lines 57-70 ("In another aspect of the present invention, the aspects comprise any one or more of functional, communication, concurrency and structural aspects of the digital system. The objects representing the functional aspects comprise any one or more of host language encapsulations, threads, and context"). Rompaey teaches that each of the hardware circuit blocks comprises:

a first processing circuit module connected to a memory for operating to selectively read or write information data from or into the memory, the first processing circuit module receiving the input packet data to read out information data needed for processing from the memory on the basis of the content of the received packet data and to output packet data obtained by adding the needed information data to the input packet data, *see* Rompaey at fig. 10;

a second processing module for receiving the packet data with the needed information data being added outputted from the first processing circuit module to create

packet data obtained by subjecting a predetermined information process to the received packet data while creating new information data, *see* Rompaey at fig. 10; and

a merging circuit module having a plurality of input terminals, to which a plurality of pieces of packet data are inputted in parallel, for outputting the plurality of pieces of packet data in serial in an inputted order without subjecting any process to the inputted packet data, *see* Rompaey at fig. 10,

wherein the information processing apparatus is configured in such a way that the input packet data is inputted from one input terminal of the merging circuit module and the output of the second processing circuit module is connected to another of the merging circuit module and that the output data from the second processing circuit module is inputted via the merging circuit module to the first processing circuit module and then new information data extracted from the output data inputted to the first processing circuit module is written into the memory while outputting the packet data subjected to the information process from the hardware circuit block, *see* Rompaey at p. 13, paragraph 3 ("A protocol may further have an index set. The indices in the index set are used to convey extra information about the data that is transported. For example the primitive protocol used to model the memory port of a processor will have an index to model the address of the data that is put on the memory port").

Regarding claims 17 and 23, Rompaey teaches an information processing apparatus comprising a plurality of hardware circuit blocks each of which is adapted to subject a specific information process to given input packet data to output processed packet data, the plurality of hardware circuit blocks mutually operating in pipeline. *See*

Rompaey at col. 6, lines 57-70 ("In another aspect of the present invention, the aspects comprise any one or more of functional, communication, concurrency and structural aspects of the digital system. The objects representing the functional aspects comprise any one or more of host language encapsulations, threads, and context"). Rompaey teaches that each of the plurality of hardware circuit modules comprises:

a first processing circuit module which operates to receive packet data and to selectively make read access or write access to a memory, *see* Rompaey at fig. 10;

a second processing circuit module for receiving packet data and information data needed to process the packet data to create packet data obtained by subjecting a predetermined information process to the packet data and to create new information data needed to process the packet data, *see* Rompaey at fig. 10; and

a merging circuit module having a plurality of parallel input terminals and a single output terminal for outputting a plurality of pieces of inputted packet from the single output terminal in inputted order without subjecting any information process to the inputted packet data, *see* Rompaey at fig. 10,

wherein the first processing circuit module selectively operates on the basis of the packet data outputted from the merging circuit module in either one of (i) a read mode in which the memory is accessed to read information data needed to process the input packet data, and (ii) a write mode in which the packet data subjected to the predetermined information process created by the second processing circuit module and the new information data to write the new information data into the memory while outputting the packet data subjected to the information process from each hardware

circuit block, *see* Rompaey at p. 13, paragraph 3 ("A protocol may further have an index set. The indices in the index set are used to convey extra information about the data that is transported. For example the primitive protocol used to model the memory port of a processor will have an index to model the address of the data that is put on the memory port").

Regarding claims 18-20, and 22, Rompaey teaches an information processing apparatus having a plurality of hardware circuit blocks constructed from software which is adapted to process input packet data on the basis of information data stored in a memory to output the processed packet data, the software comprising (i) a first function in which the input packet data is received, information data needed to process the received packet data is read out of the memory and the input packet data is returned together with the information data, (ii) a second function in which a predetermined information process is subjected to the-input packet data on the basis of a result of the process by the first function while creating new information data, and (iii) the information data stored in the memory rewritten on the basis of a result of the process by the second function and the content to packet data be outputted is returned. *see* Rompaey at col. 6, lines 18-34 (describing how hierarchal objects combine primitive components); Rompaey at fig. 10; Rompaey at p. 13, paragraph 3 ("A protocol may further have an index set. The indices in the index set are used to convey extra information about the data that is transported. For example the primitive protocol used to model the memory port of a processor will have an index to model the address of the data that is put on the

memory port"). Rompaey teaches that each of the plurality of hardware circuit blocks comprises:

a first hardware module capable of selectively executing either the process by the first function or the process by the third function in response to the input packet data and on the basis of the content thereof, *see* Rompaey at fig. 10;

a second hardware module capable of executing the process by the second function, *see* Rompaey at fig. 10; and

an interface for receiving in parallel the input packet data and the packet data outputted from the second hardware module and for sequentially outputting these packet data to transfer the outputted packet data to the first hardware module, *see* Rompaey at fig. 10.

4. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Rompaey** in view of **Official Notice**.

Regarding claim 21, Examiner takes Official Notice that functionality for an internet server and for data mining, natural language processing, network information processing, DNA computation and simulation, physical simulation, and audio/video processing are well known in the art. It would have been obvious to one of ordinary skill in the art to use Rompaey's process to implement any of these applications because Rompaey teaches that the disclosed process makes the application hardware design more efficient. *See generally* Rompaey at col. 5-6.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLOW NOONAN whose telephone number is (571)270-1322. The examiner can normally be reached on Monday through Friday, 7:30 AM-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W. N./
Examiner, Art Unit 2146

/Jeffrey Pwu/
Supervisory Patent Examiner, Art Unit 2146